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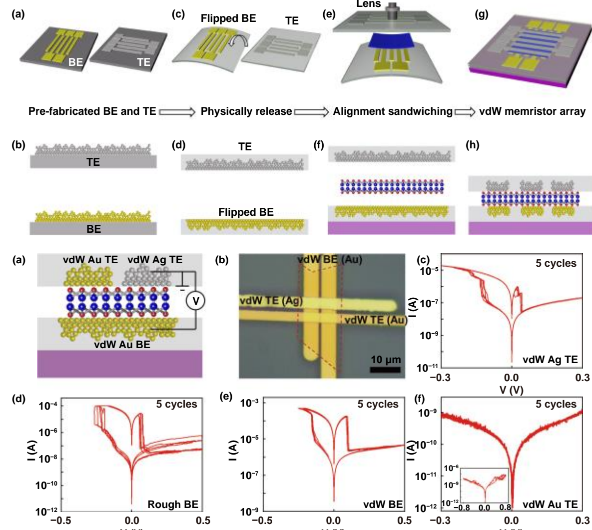
Low voltage and robust InSe memristor using van der Waals electrodes integration

Qianyuan Li, Quanyang Tao, Yang Chen, Lingan Kong, Zhiwen Shu, Huigao Duan, Lei Liao and Yuan Liu

Highlights:

- A van der Waals (vdW) memristor by physically sandwiching pre-fabricated metal electrodes on both sides of the two-dimensional channel material is demonstrated for the first time.
- The memristor arrays shows a high integration density of 10^{10} cm^{-2}, a high stability and the lowest set/reset voltage of 0.12V/0.04V, which is a record low value for all 2D-based memristors.
- The improved memristor behavior is confirmed the result of optimized BE/channel and TE/channel interfaces.
- A general electrode integration approach is provided for other 2D memristors which have previously been limited by non-ideal contact integration, high operation voltage and poor device stability.



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Low voltage and robust InSe memristor using van der Waals electrodes integration

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Abstract

Memristors have attracted tremendous interest in the fields of high-density memory and neuromorphic computing. However, despite the tremendous efforts that have been devoted over recent years, high operating voltage, poor stability, and large device variability remain key limitations for its practical application and can be partially attributed to the un-optimized interfaces between electrodes and the channel material. We demonstrate, for the first time, a van der Waals (vdW) memristor by physically sandwiching pre-fabricated metal electrodes on both sides of the two-dimensional channel material. The atomically flat bottom electrode ensures intimate contact between the channel and electrode (hence low operation voltage), and the vdW integration of the top electrode avoids the damage induced by aggressive fabrication processes (e.g. sputtering, lithography) directly applied to the channel material, improving device stability. Together, we demonstrate memristor arrays with a high integration density of 10^{10} cm^{-2}, high stability, and the lowest set/reset voltage of 0.12 V/0.04 V, which is a record low value for all 2D-based memristors, as far as we know. Furthermore, detailed characterizations are conducted to confirm that the improved memristor behavior is the result of optimized metal/channel interfaces. Our study not only demonstrates robust and low voltage memristor, but also provides a general electrode integration approach for other memristors, such as oxide based memristors, that have previously been limited by non-ideal contact integration, high operation voltage and poor device stability.

Keywords: 2D-material, robust memristor, ultra-low threshold, atomically flat interfaces

1. Introduction

Memristors have attracted considerable attention for neuromorphic computing [1–6] and high-density memory [7–12]. However, despite the tremendous efforts devoted over recent years, the poor stability [6, 13] and large device variability [14, 15] remain key limitations for its practical application. Although the cell-to-cell variability can be addressed with more controllable fabrication conditions (e.g. industry-compatible processing line), the large cycle-to-cycle variability is intrinsically inherited from the device structure and can be partially attributed to the non-ideal interfaces between the metal electrodes and the active channel. From the structural point of view, a typical vertical memristor has a three-layer metal/channel/metal sandwich structure with two interfaces:

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the bottom electrode (BE)/channel interface and the top electrode (TE)/channel interface, both of which are imperative for device operation and could greatly impact memristor reproducibility and stability. For example, noble metals (e.g. Au, Pt) favor the formation of isolated islands or percolated networks during initial substrate deposition, leading to a BE surface roughness ~1–3 nm, which can further increase to tens or hundreds of nanometers after the BE annealing process [16]. Such a rough BE/channel interface results in non-uniform channel materials with localized strain, random band-structures, and electrical properties, leading to a variable electrical field distribution and large cycle-to-cycle variability. On the other hand, conventional TE metals are fabricated through direct deposition techniques based on the vaporization of precursor materials (e.g. thermal/e-beam evaporation or sputtering) and usually involve repeated bombardment by high-energy hot metal atoms or atomic clusters, resulting in considerable interface damage, metal diffusion into the channel [17], and non-repeatable device behavior. This TE contact damage is particularly fatal for ultra-thin vertical memristors where the TE contact region is essentially the entire channel, leading to greatly enhanced leakage current, device instability, and eventually device failure.

Various efforts have been devoted to improving memristor stability, cycling endurance, and parameter reproducibility. Early attempts used a buffer layer to construct a bilayer channel structure with improved stability and performance [18–20]. For example, an intermediate HfO_X layer between the TE metal and HfO_2 active channel was demonstrated to significantly influence the switching behavior and was an essential part of reliable device operation, where the intermediate suboxide mediated oxygen ion movement, serving as a buffer for redox reactions. However, the insertion of an oxide buffer could increase the device's overall resistance with high set/reset voltage over 3 V/1.6 V [19]. Alternatively, robust memristor operation was demonstrated by using a two-dimensional (2D) semiconductor MoS_2 as the active channel and 2D graphene as both the TE and BE [21]. The dangling-bond free 2D surface (MoS_2 and graphene) offers atomically sharp and clean interfaces within the TE/channel and BE/channel interfaces [22], overcoming previous limitations from BE roughness and TE deposition induced damage, hence demonstrating improved device stability with working temperatures over 340 °C. Nevertheless, the relatively low conductivity of graphene electrodes leads to excess series resistance, and the inert graphene electrodes prohibit the low voltage electrochemical metallization (ECM) mechanism, limiting the set/reset voltage to 1.2 V/1.1 V. The resistance limiting effect may become more pronounced with increasing integration density by reducing the graphene electrode width (e.g. scaled below 100 nm into graphene nanoribbons).

Here, we demonstrate a new approach for low voltage and robust memristor operation by using InSe as the active channel and damage-free van der Waals (vdW) metals as both the BE (Au) and TE (Ag). By mechanically laminating and sandwiching prefabricated metal electrodes with atomically flat surfaces on both sides of an ultra-thin InSe, the intrinsic channel material can be well retained without conventional metal deposition induced damage. More importantly, the interfaces of both the BE/channel and TE/channel are atomically clean and sharp, overcoming the previous limitations of poor interface quality (e.g. point-contact, inhomogeneous channel), hence, leading to improved device stability and reduced operation voltage. Together, we demonstrate memristor arrays with a high integration density of 10^{10} cm^{-2}

and operation duration over 400 cycles, which is a four-fold increase compared to the control sample using conventional deposited BE and TE. Notably, with desired vdW metal/channel interfaces, the channel thickness can be scaled to 1.6 nm with an ultra-low set/reset voltage of 0.12 V/0.04 V, which is a record low value for 2D based memristors, to the best of our knowledge. Furthermore, detailed characterizations are conducted to investigate the impact of BE roughness and TE deposition induced damages, confirming that the improved memristor behavior is the result of optimized metal/channel interfaces in both BE and TE. Our study not only demonstrates a reliable and low voltage memristor, but also provides a general electrode integration approach for other memristors or other ultra-thin vertical devices that are previously limited by non-ideal contact integration and poor device stability.

2. Results and discussion

2.1. Fabrication flow of vdW memristors

Figure 1 schematically illustrates the process flow for fabricating our memristor with both vdW TE and BE contact. First, Au and Ag (both 50 nm thick) metal electrode arrays are prefabricated on two separate Si substrates, as shown in figures 1(a) and (b). They can be mechanically released from the substrate using a previously developed method [23] and demonstrate an atomically flat surface, replicating the flat surface of the silicon substrate (details in the Methods section). Next, the released Au electrode arrays (used as BE) are flipped and placed on a SiO_2 substrate, where the flat surface is facing up, as schematically shown in figures 1(c) and (d). In this way, we achieved flat BE arrays to overcome the previous limitation of surface roughness. Then, a few layers of InSe flake are used as the channel material and integrated on top of the BE arrays using a standard dry alignment transfer process, forming an intimate contact with the BE and a uniform Au/InSe interface (figures 1(e) and (f)). Finally, the previously released Ag electrode arrays are mechanically laminated on top of the InSe channel as the TE contact, forming a crossbar structure with the BE, as shown in figures 1(g) and (h). Notably, the vdW integration process of the TE also leads to an atomically clean and electrically sharp TE/InSe interface, which is essential to maintain the intrinsic properties of the ultra-thin channel and to improve the device's overall uniformity and reproducibility. This is in significant contrast to the conventional TE direct deposition process, which involves repeated bombardment of the channel by high-energy hot atoms or atomic clusters,

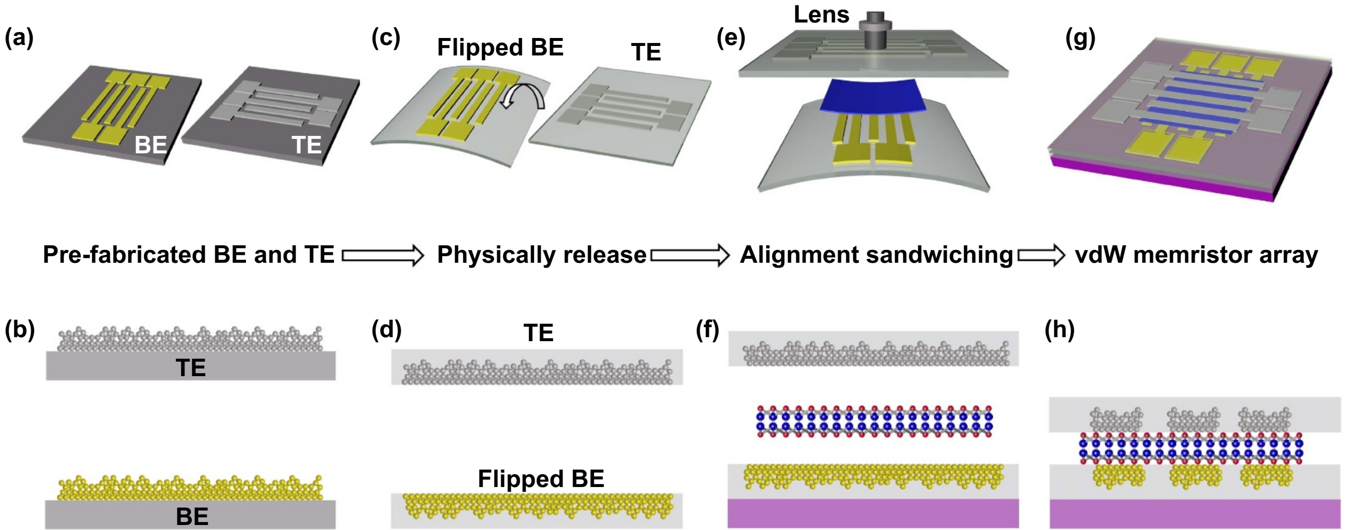

Figure 1. (a), (b) Perspective (a) and cross-sectional (b) schematics of prefabricated BE and TE arrays on two separated silicon substrates; (c), (d) perspective (c) and cross-sectional (d) schematics of the released BE and TE arrays. The released BE arrays are flipped with the atomically flat surface; (e), (f) perspective (e) and cross-sectional (f) schematics of the alignment sandwiching process of the BE, InSe, and TE under an optical microscope; (g), (h) perspective (g) and cross-sectional (h) schematics of the vdW memristor arrays with atomically flat interfaces.

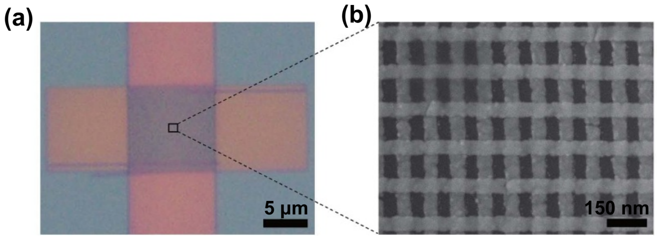

Figure 2. Optical image (a) and scanning electron microscope image (b) of memristor arrays with 50 nm electrode width and 100 nm pitch size. Thickness of electrodes is 20 nm.

leading to considerable interface damage, metal diffusion into the channel [17, 24], and non-repeatable device behavior, particularly in ultra-thin channels.

Using the above fabrication process, we achieved memristor crossbar arrays with the intrinsic 2D channel sandwiched between two flat metals based on physical lamination processes. We note that the demonstrated vdW electrode lamination processes (of both TE and BE) are compatible with high density crossbar memristors. Figure 2 shows memristor arrays with 50 nm line width and 100 nm pitch size (the size of the array is dependent on the exfoliated film), corresponding to a high integration density of 10^{10} cm^{-2}. Further reducing the pitch size can lead to the contact between two neighbor electrodes (and device short) due to the strain generated during the vdW integration process.

2.2. Electrical performance and the memristive mechanism

Electrical transport studies of the vdW memristor are carried out at room temperature in a Lakeshore probe-station under vacuum conditions (10^{-5} torr). For the measurement of all devices, the TE is grounded, and the BE is always biased (figures 3(a) and (b)). As shown in figures 3(c), a vdW memristor with a bilayer InSe channel (1.6 nm thick) exhibits bipolar resistive switching and nonvolatile behavior with the lowest set/reset voltages at 0.12 V/0.04 V, which is the lowest recorded value of all 2D-based memristors. The observed low switching voltages are important for neuromorphic computing and can be largely attributed to several geometric advantages of our vdW structure. First, the vdW integration of TE metals minimizes conventional fabrication induced damage to channel material, enabling a highly scaled channel thickness of 1.6 nm while retaining intrinsic channel properties. The ultra-thin body thickness is crucial to reduce the bias voltage required for Ag filament formation and then the reduced set/reset voltage [25]. On the other hand, the atomically flat BE surface ensures intimate BE/channel contact with low contact resistance in contrast to the conventional rough BE with a much smaller metal-2D contact area (point-like contact in rough BE/channel interface) with higher contact resistance, as shown in figures 3(d) and (e). The low BE contact resistance reduces the undesired voltage drop in the contact region and further decreases the overall set/reset voltage. Furthermore, the vdW metal electrode's (Ag or Au) contact resistance shows lower series resistance compared to previously used graphene electrodes [21], which also helps to reduce undesired voltage drop.

Beyond the vdW interfaces, the use of Ag as the TE metal is another important contributing factor for the low set/reset voltage achieved. Owning to the active nature of Ag atoms, our vdW memristor can be an ECM device, whereas previous memristors based on layered MoS_2 channels are more likely to be valence change memory (VCM) devices [21, 26]. ECM devices generally exhibit lower operation voltage [27] due to the lower energy required for metal filament formation. To

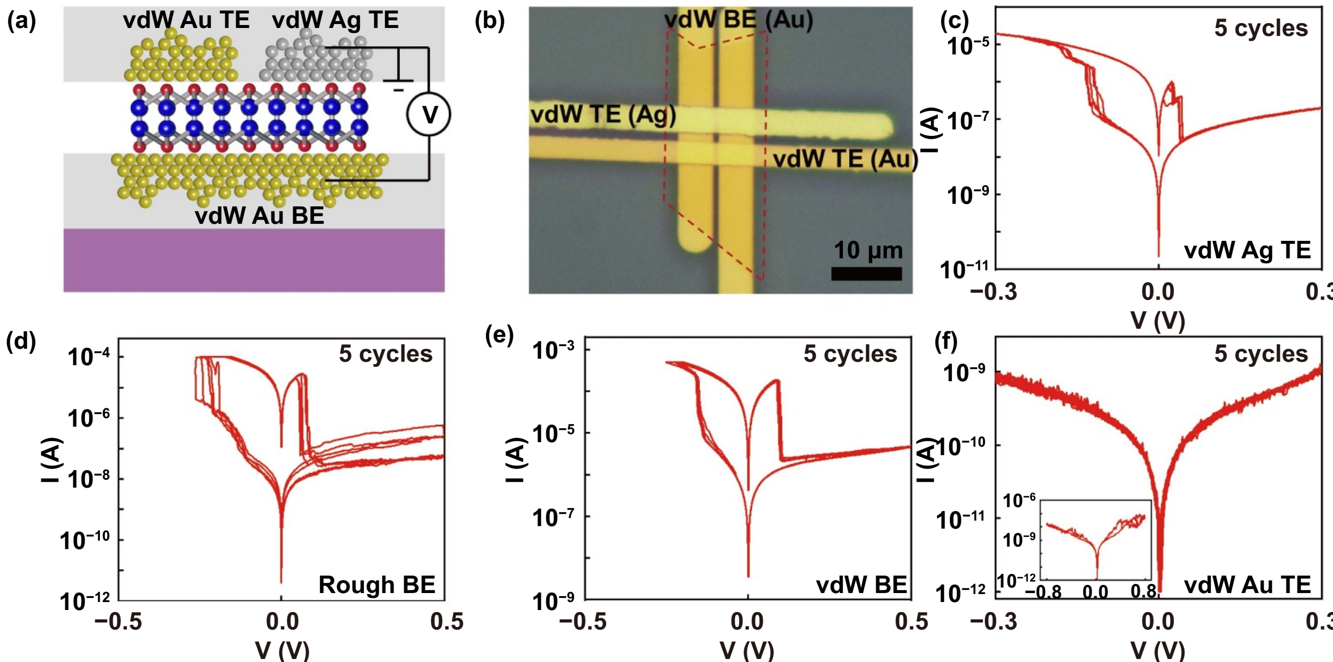

Figure 3. (a), (b) Schematic illustration (a) and optical image (b) of two parallel vdW memristors on the same InSe flake. These devices are fabricated using the same batch of processes, where the TE is Ag in one device and Au in another device. The red dashed line represents the bilayer InSe flake; (c) *I–V* curve of vdW Ag/InSe/Au memristor with clear switching behavior and low operation voltage; (d), (e) memristor performance using rough BE and vdW BE, respectively; (f) *I–V* curve of parallel vdW Au/InSe/Au device without any resistive switching behavior, suggesting the ECM mechanism of our vdW memristor. The insert is the output curve while bias voltage increases to 0.8 V.

confirm the ECM working mechanism in our devices, another parallel Au TE is vdW integrated on the same InSe/BE heterostructures using the same batch of fabrication (figures 3(a) and (b)). As shown in figure 3(f), the control device (Au/InSe/Au) does not demonstrate any resistive switching behavior even bias increases to 0.8 V. This is in contrast to the preferred memristive behavior within the parallel Ag/InSe/Au vdW structure, suggesting the Ag electrode is essential for memristor operation, consistent with previous ECM mechanisms based on Ag filament formation [28].

2.3. Comparison of memristors with rough BE and vdW flat BE

To further investigate device stability and demonstrate the importance of the vdW BE/channel interface, we fabricated memristors using both evaporated rough BE and vdW flat BE, while increasing the channel thickness to 2.4 nm and using vdW Ag TE consistently. First, atomic force microscopy is conducted to characterize the surface morphology of both BEs after integrating the InSe channel. As shown in figure 4(a), the vdW Au BE demonstrates an atomically flat surface with a root mean square (RMS) roughness of 0.27 nm. Importantly, the RMS remains unchanged after integrating the InSe channel, suggesting intimate contact between the BE/channel interface, as schematically illustrated in figure 4(a). Conversely, the as-deposited Au BE shows rough surface with a large RMS of 1.1 nm, which is consistent with previous reports [29]. In particular, the surface RMS reduces to 0.6 nm after integrating the InSe channel on top of this rough BE (figure 4(b)), indicating the InSe channel does not follow the surface morphology of the underlying BE and poor contact (i.e. insufficient and localized contact area) within the conventional BE/channel interface, as schematically illustrated in figure 4(c). Such a rough BE/channel interface results in non-uniform channels with localized strain and random band structures and channel conductivity, leading to variable electrical field distribution and large cycle-to-cycle variability (figure 4(d)). Based on the measurement of the first 50 cycles, the device with rough BE demonstrates highly variable switching behavior. As shown in figures 4(e) and (f), resistances of the high resistance state (HRS) and the low resistance state (LRS) are randomly distributed in the range of 10^3 Ω to 10^8 Ω with 5 orders of magnitude of variation. Similarly, the set/reset voltage shows large variation between 0.1 V and 0.5 V.

In contrast, devices with vdW flat BE demonstrates significantly less cycle-to-cycle variability. As shown in figure 4(g), the multicycle measurement exhibits nearly identical characteristics. The extracted HRS and LRS resistances remains relatively stable and demonstrate similar values within first 50 cycles. Furthermore, the set/reset voltage is distributed in much narrower ranges of 0.15 V to 0.25 V and 0.04 V to 0.09 V (figures 4(h) and (i)), respectively, which are nearly an order of magnitude improvement compared to the device with rough BE. Moreover, after 400 cycles, the device still demonstrates a uniform memristor phenomenon while the rough BE device fails to switch resistance after 100 cycles, as shown in figure 5. The above comparisons clearly illustrate the importance of

Figure 4. (a), (b) AFM characterizations and schematics of vdW BE (a) and conventional deposited BE (b) after integrating the InSe channel. In particular, the RMS roughness of deposited BE in red dashed line reduces from 1.1 nm to 0.6 nm by integrating InSe, suggesting poor BE/channel contact. Scale bars are 0.5 μm; (c), (d) schematic and *I–V* measurement of the control device with rough BE/channel interface; (e), (f) distribution statistics of HSR/LSR resistance (e) and set/reset voltage (f) with 50 cycles, where large device variations are observed; (g)–(i) electrical properties of a vdW memristor (with flat BE surface) with 50 cycles, demonstrating smaller device variations and suggesting the importance of the BE/channel interface.

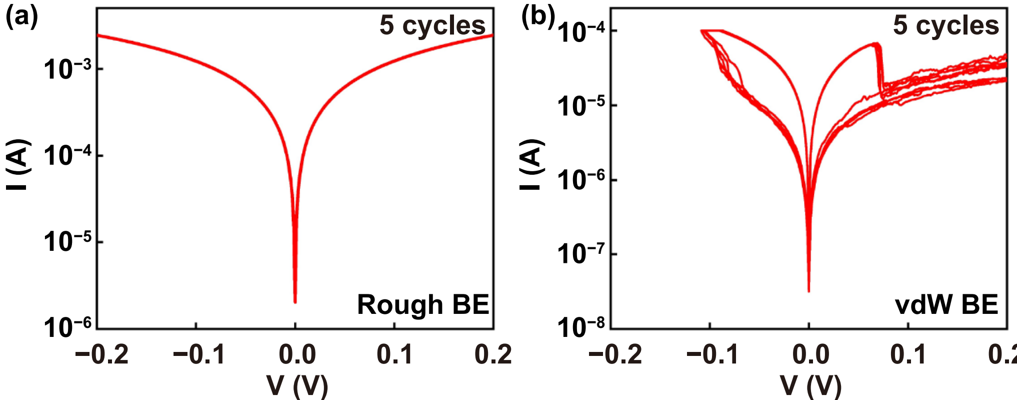

Figure 5. (a) *I–V* curve of memristor with rough BE after 100 cycles measurement, where the linear curve is always observed, suggesting device failure; (b) *I–V* curve of the memristor with vdW BE after 400 cycles measurement, where the memristor behavior is well-retained.

BE surface roughness for device stability and suggest that the vdW flat BE is essential for stable memristor operation. Furthermore, we note that the integration of an atomically flat BE for other oxide-based memristors [30, 31] or organic based memristors [32] would be an interesting topic for future investigation.

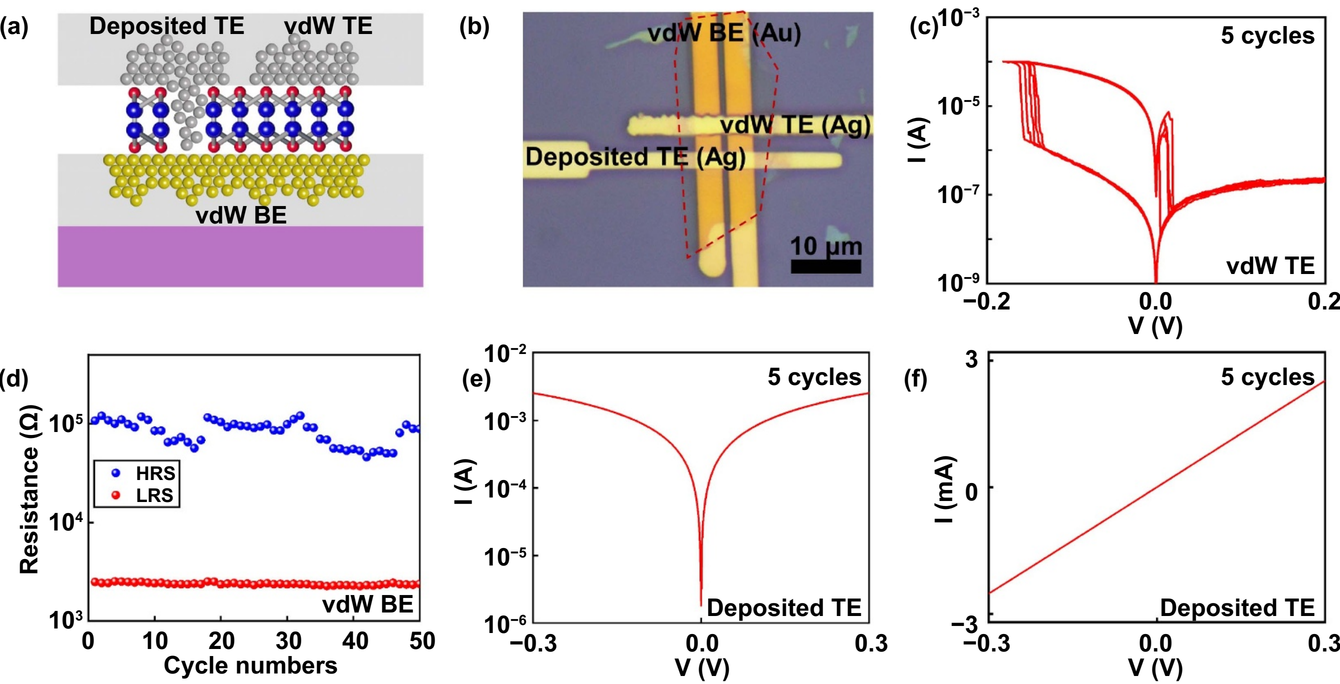

Figure 6. (a), (b) Schematic and optical image of the devices on the same InSe flake, where the TE of one device is vdW integrated and another is directly deposited. Red dashed line represents the 3.2 nm thick InSe flake; (c), (d) *I*–*V* curve and the distribution statistics of the device with vdW TE, demonstrating desired memristor behavior; (e), (f) Electrical measurement of the parallel device with directly deposited TE, showing the short-circuit and suggesting that conventional TE fabrications induce considerable damage.

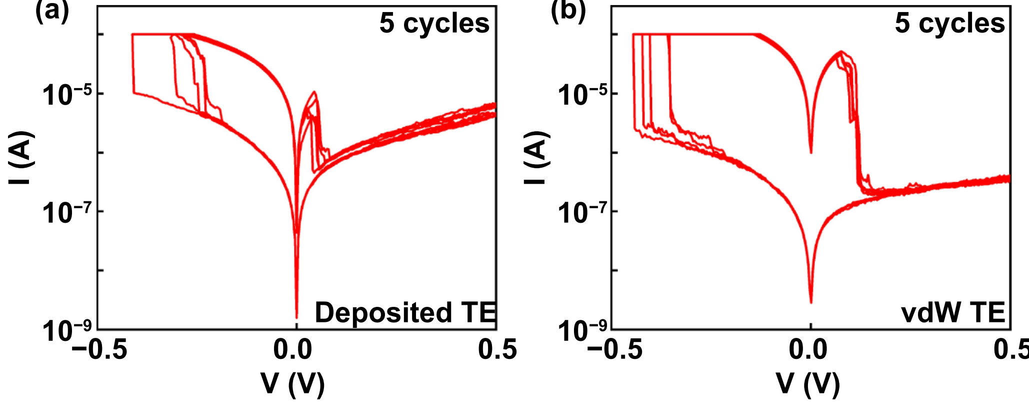

Figure 7. (a), (b) *I*–*V* output curves of memristors with deposited TE (a) and vdW TE (b), where clear switching behavior is observed in both devices with 6.4 nm channel thickness.

2.4. Comparison of memristors with high-energy deposited TE and low energy vdW TE

Finally, in order to investigate the impact of TE to memristor reproducibility and stability, we fabricated Ag/InSe/Au devices using conventional deposited Ag TE as well as our vdW integrated Ag TE on the same InSe flake, as shown in figures 6(a) and (b). The detailed device fabrication process is described in the Methods section. An atomically flat BE is consistently used in both devices to provide a fair comparison. As shown in figure 6(c), the device with vdW TE demonstrates robust and low voltage memory behavior within multi-cycle measurements. Figure 6(d) further summarizes the HRS/LRS resistance distribution, which demonstrates uniform device operation consistent with the previous electrical measurement in figure 4. In contrast, the memristor behavior is totally lost in the control device that uses conventional directly deposited TE on the same InSe flake, as shown in figures 6(e) and (f). During multi-cycle measurements, the as-fabricated device always exhibits a linear *I*–*V* curve with low resistance ($\sim$100 Ω), suggesting a short circuit between TE and BE. This could be largely attributed to the conventional aggressive TE fabrication process directly performed on the channel material (e.g. high-energy lithography, wet-chemical development, and high temperature metal deposition), leading to considerable damage and metal diffusion into the channel material as have been characterized through transmission electron microscopy

(TEM) in previous literature [17] and schematically illustrated in figure 6(a).

We note that the TE deposition induced damage and device failure become more pronounced when scaling the channel thickness. For all devices with channel thickness below 3.2 nm, the device failure (short circuit) and linear *I–V* curve are consistently observed when using directly deposited TE, without any memristor behavior, limiting device thickness scaling to low voltage applications. While the channel thickness increases beyond 6.4 nm, devices using deposited TE re-exhibit memristor behavior, as shown in figure 7. However, large cycle-to-cycle variation (over 0.2 V) and smaller HRS/LSR ratio (over 10) are still observed within these devices, further confirming the unoptimized device behavior using directly deposited TE techniques.

3. Summary

In conclusion, we demonstrated a vdW memristor by physically sandwiching pre-fabricated electrode arrays on both sides of an InSe channel. The fabricated device shows high integration density, high device stability, and low operation voltage compared to the device fabricated using conventional rough BE or directly deposited TE. Furthermore, detailed characterizations were conducted to confirm that the improved memristor behavior resulted from the optimized BE/channel and TE/channel interfaces. Our study not only demonstrates a robust InSe memristor with the lowest operation voltage, but also provides a general electrode integration approach for 2D memristors. It may also provide exciting implications for oxide-based memristors or other ultra-thin electronic devices that are limited by poor device stability or non-ideal interfaces.

4. Methods

4.1. Fabrication process of vdW electrodes memristors

First, 50 nm thick Au electrode arrays (used as BE) and 30 nm/20 nm thick Ag/Au electrode arrays (used as TE) are thermally deposited onto two separate sacrificial silicon substrates with atomically flat surfaces. Next, 500 nm thick polymethyl methacrylate is spin-coated on the pre-fabricated electrode arrays after hexamethyldisilazane treatment [17], working as a protection layer. Au electrodes are then mechanically released and flipped upside down, so the atomically flat surface faces up, as schematically illustrated in figures 1(c) and (d). Finally, a few layers of InSe flake (mechanically exfoliated for all devices) and Ag/Au electrodes (released from another substrate using the above approach) are successively vdW integrated onto the flat surface, to form the vdW memristor structure.

4.2. Fabrication of memristor with parallel vdW TEs using Ag and Au metal

To fabricate the control device with both Ag and Au electrodes in figure 3, asymmetric electrodes pair are pre-fabricated on a sacrificial silicon substrate using two times thermal deposition, where one electrode consists of 50 nm thick Au and the other consists of 30 nm/20 nm thick Ag/Au. The pair of asymmetric electrodes are released and physically laminated on top of a BE/InSe heterostructure, forming two parallel vdW memristors (one Ag/InSe/Au and the other Au/InSe/Au) on the same InSe flake.

4.3. Fabrication of memristor with deposited and vdW TEs

To fabricate the control device with both deposited and vdW TE in figure 6, a few layers of InSe are first exfoliated on a SiO_2 substrate. A 30 nm/20 nm thick Ag/Au electrode is then vdW integrated on the InSe channel using the previously described method. Next, another parallel electrode (also 30 nm/20 nm thick Ag/Au) is directly deposited on the same InSe flake using vacuum thermal evaporation. Finally, the InSe channel with two different electrodes is transferred on top of a BE with an atomically flat surface, as shown in figures 6(a) and (b). Using this approach, we achieved control over memristors on the same InSe channel, with one vdW TE and another directly deposited TE.

4.4. Electrical measurement

Electrical transport studies of all memristors are carried out at room temperature in a Lakeshore PS-100 cryogenic probe station under vacuum conditions (10^{-5} torr), using Keysight B2900A source measurement unit.

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Author contributions

Y L conceived the research. Y L and Q L designed the experiments. Q L fabricated the samples and performed the device measurement. Q T, L K, Y C and L L contributed to the discussion of results and manuscript editing. Z S and H D aided in fabricating the high-density electrode arrays. Y L and Q L co-wrote the manuscript. All authors discussed the results and commented on the manuscript.

Conflict of interest

The authors declare no competing interests.

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